

**AMENDMENTS TO THE CLAIMS**

Please amend claims 1, 4, 5, 20, 22, 23 and 24 as follows.

Please cancel claims 2, 3, 21, 25 and 26.

1. (Currently amended) A die, comprising:
- a dielectric layer positioned on top of a semiconductor support layer;
- a via passing through the dielectric layer and the semiconductor support layer,
- wherein a first end of the via is positioned in the dielectric layer and a second end of the via is positioned in the semiconductor support layer, wherein a first diameter of the first end is greater than a second diameter of the second end, wherein the second end of the via includes a shaft, the shaft including a shaft diameter similar to the second diameter, wherein the shaft tapers outward from a center of the via within the semiconductor support layer toward the dielectric layer to form a semi-cone shape in the semiconductor support layer, wherein the semi-cone shape forms an increased via contact area at the first end for coupling the via to the contact; and

a contact positioned on top of the dielectric layer, the contact coupled to the first end of the via, ~~wherein the contact to be coupled to a device of the die.~~

2. (Cancelled)

3. (Cancelled)

Atty Docket: 42P16903

Serial No. 10/674,704

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4. (Currently amended) The die of claim 1 wherein the via continues to taper outwards from the second end into the first end to form a semi-cone shape in the dielectric layer.
5. (Currently amended) The die of claim 1 wherein a diameter of the first end is similar to a diameter of the semi-cone shape, the first end to form a cylinder shape in the dielectric layer.
6. (Cancelled)
7. (Previously Presented) The die of claim 1 wherein the via includes a metal-filled via.

Claims 8-19 (Cancelled).

20. (Currently amended) A die package, comprising:
- a semiconductor support layer;
  - a dielectric layer disposed on the semiconductor support layer;
  - a via including a first end and a second end, the first end positioned in the dielectric layer and the second end positioned in the semiconductor support layer, wherein a diameter of the first end is greater than a diameter of the second end, wherein the second end includes a shaft and an enlarged end, the enlarged end between the shaft and the first end, wherein the enlarged end tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer, the enlarged end defining a semi-cone shape, wherein the

enlarged end creates an increased via contact area at the first end for coupling the via to the first contact;

a first contact, disposed on the dielectric layer, coupled to the first end of the via;  
~~wherein the first contact coupled to a device of a die of the die package; and~~

a second contact, disposed on the semiconductor support layer, coupled to the second end of the via, wherein the second contact to be mounted to a printed circuit board.

21. (Cancelled)

22. (Currently amended) The die package of claim ~~20~~ 21 wherein the first end continues to taper outwards from the enlarged end to form a semi-cone shape in the dielectric layer.

23. (Currently amended) The die package of claim ~~20~~ 21 wherein a diameter of the first end of the via through the dielectric layer is similar to a diameter of the semi-cone shape, the first end to form a cylinder shape in the dielectric layer.

24. (Currently amended) A system, comprising:

a printed circuit board (PCB); and

a processor coupled to the PCB, wherein the processor includes:

a dielectric layer positioned on top of a semiconductor support layer;

a via passing through the dielectric layer and the semiconductor support layer, wherein a first end of the via is positioned in the dielectric layer and a second end of the via is positioned in the semiconductor support layer,

wherein a first diameter of the first end is greater than a second diameter of the second end, wherein the second end includes a shaft, the shaft including a shaft diameter similar to the second diameter, wherein the second end tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer, the second end defining a semi-cone shape on the semiconductor support layer; and

a first contact positioned on top of the dielectric layer, the first contact coupled to the first end of the via, ~~wherein the first contact is coupled to a device of the processor;~~

wherein the second end of the via is coupled to the PCB via a second contact.

25. (Cancelled)

26. (Cancelled)

27. (Original) The system of claim 24 wherein the first diameter is approximately twice the second diameter.